REMARKS

Applicants acknowledge the stated allowance of claims 4-15.

By this Amendment, Applicants amend claim 1.

Accordingly, claims 1-21 remain pending in the application.

Reexamination and reconsideration are also respectfully requested in view of the following Remarks.

35 U.S.C. § 103

The Office Action rejects claims 1-3 and 16-21 under 35 U.S.C. § 103 over Williams et al. U.S. Patent 5,485,027 ("Williams").

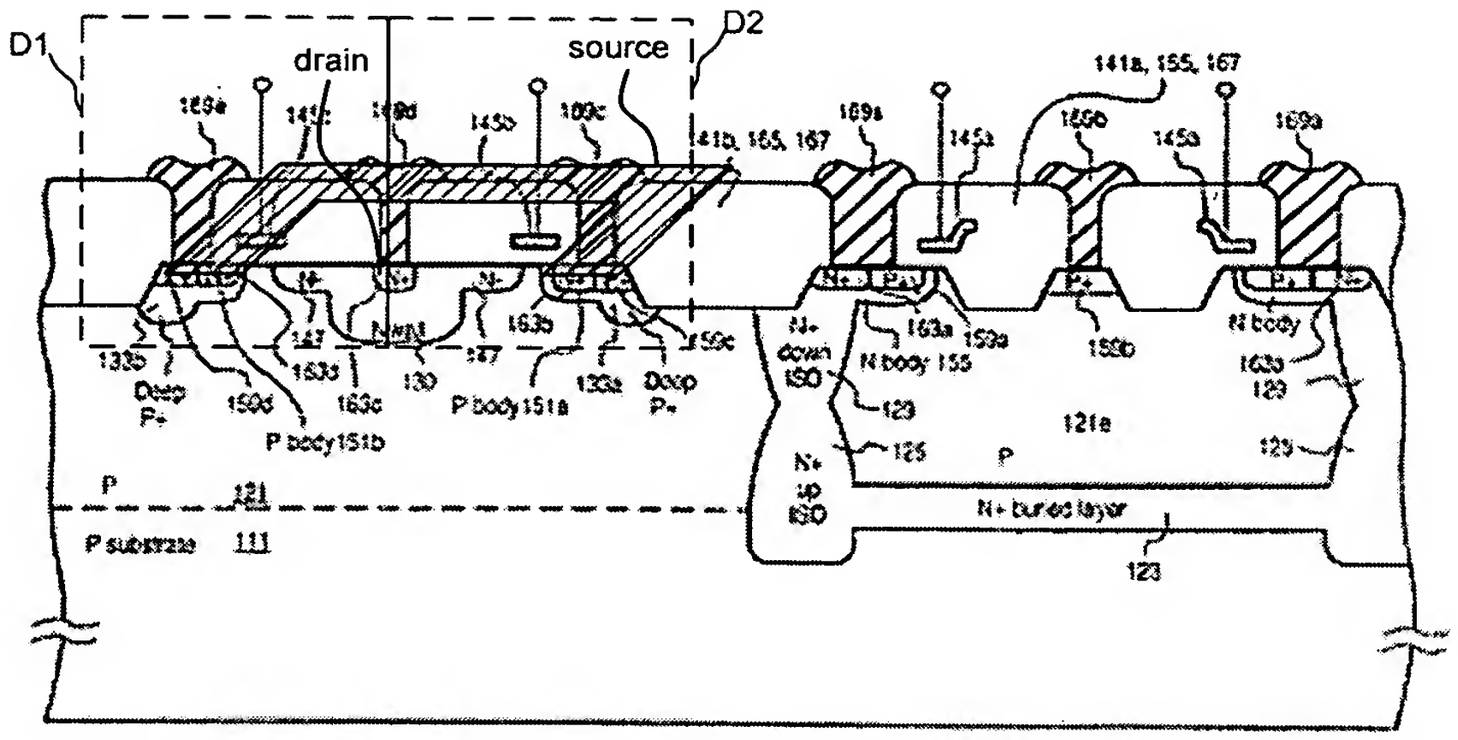
Applicants respectfully submit that claims 1-3 and 16-21 are patentable over Williams for at least the following reasons.

Claim 1

Among other things, the array of claim 1 includes N DMOS transistors laterally arranged in an epitaxial layer, wherein each DMOS transistor has a source and a drain, wherein either the source or the drain surrounds the other.

Applicants respectfully submit that Williams does not disclose N DMOS including such a combination of features.

William discloses that it is optional whether the gate and source also surround the drain and form a familiar "annular device" (Williams, paragraph 1, lines 50-55). However, in Williams, unless the sources 163b and 163d are connected to each other, one of the sources 163b and 163d is formed unique to each transistor D1 and D2, and the drain 163c is shared commonly to the transistor D1 and D2 (see Figure A below). However, if the sources 163b and 163d surround the drain 163c, as noted above Williams teaches that the DMOS transistor is the cylindrically shaped "annular device," and therefore Williams cannot teach **a plurality of DMOS transistors laterally arranged in an epitaxial layer**, wherein each DMOS transistor has a source and a drain, **wherein either the source or the drain surrounds the other** as recited in claim 1.



Therefore, Williams can not and does not disclose a plurality of DMOS transistors laterally arranged wherein each transistor includes a source and a drain, wherein one of the source and drain surrounds the other.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over Williams.

Claims 2-3 and 16-20

Claims 2-3 and 16-20 depend from claim 1 and are therefore deemed patentable over Williams for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 2

In claim 2, the DMOS transistors laterally arranged in the epitaxial layer are N-type vertical double diffused MOS transistors (nVDMOS transistors).

Applicants respectfully submit that Williams fails to disclose an array including such a combination of features. The Office Action states that Williams disclose that vertical and lateral type devices may be employed. Of course, that is not what is specifically recited in claim 2. FIG. 7 of Williams discloses vertical DMOS devices. However, the vertical DMOS devices of FIG. 7: (1) are not laterally arranged in the epitaxial layer; and (2) do not share in common either a source or drain.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 2 is patentable over Williams.

Claim 16

Among other things, in the array of claim 16 one of the source or drain commonly shared among the N DMOS transistors surrounds the one of the source or drain of each double diffused MOS transistor formed unique to each DMOS transistor.

Applicants respectfully submit that no such feature is disclosed by Williams. The Office Action cites FIGs. 2, 5, 23 and 25O. However, Williams never discloses or suggests with respect to FIGs. 2, 5, 23 and 25O that a source or drain commonly shared among N DMOS transistors surrounds a source or drain of each of the N DMOS transistors, that is formed unique to each DMOS transistor.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 16 is patentable over Williams.

Claim 21

Among other things, the array of claim 21 **three or more** double diffused MOS transistors (DMOS transistor) are laterally arranged in the epitaxial layer, wherein one of a source or drain of each of the three or more double diffused MOS transistor is formed unique to each transistor, and wherein the three or more DMOS transistors share in common the other of the source or drain.

Applicants respectfully submit that the cited prior art does not disclose or suggest an array including these features in combination with the other features of claim 1 from which claim 21 depends. Specifically, the array of claim 21 includes **three of more DMOS transistors commonly sharing one source or drain**. This is not possible with any of the various layouts disclosed in Williams. Furthermore, Williams gives no suggestion in his various layouts as to how one would even go about producing a structure where three of more DMOS transistors commonly share one source or drain.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 21 is patentable over Williams.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-21, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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By: _____
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